WHAT IS CLAIMED IS:

1. A computer-implemented method for facilitating physical synthesis of a circuit design, the circuit design comprising a plurality cell instances organized hierarchically, each cell instance corresponding schematically to one of a plurality of cell types, the method comprising:

sizing transistors in each of the cell instances with reference to an objective function thereby resulting in a first plurality of cell subtypes for each cell type, each cell subtype corresponding to a particular cell type differing from all other cell subtypes corresponding to the particular cell type by at least one transistor dimension; and

merging selected ones of the subtypes for at least one of the cell types thereby resulting in a second plurality of subtypes for the at least one of the cell types, the second plurality of subtypes being fewer than the first plurality of subtypes, wherein merging of the selected subtypes achieves a balance between the objective function and a cost associated with maintaining the selected subtypes distinct.

2. The method of claim 1 further comprising partitioning the cell instances for each cell type into at least one instance class, the cell instances in each instance class having a same relationship to an immediate parent cell, each instance class corresponding to one of the first plurality of subtypes.

3. The method of claim 2 wherein the partitioning of the cell instances is performed with reference to at least one user-defined constraint.

4. The method of claim 2 wherein the partitioning of cell instances is performed prior to the sizing of the transistors.

5. The method of claim 2 wherein the partitioning of cell instances is performed after the sizing of the transistors.

6. The method of claim 2 wherein the merging of the selected subtypes is performed with reference to the instance classes.

7. The method of claim 1 wherein the circuit design corresponds to an asynchronous circuit.

8. The method of claim 1 wherein the circuit design corresponds to a synchronous circuit.

9. The method of claim 1 wherein the merging of the selected subtypes is performed with reference to a distance function which represents a distance between two of the selected subtypes in a metric space which relates the objective function and the cost.

10. The method of claim 9 wherein the distance function comprises a plurality of components which includes any of a layout cost corresponding to the selected subtypes, a number of instances of each of the selected subtypes, transistor sizes for the selected subtypes, estimated transistor sizes for a merged subtype, external resistive loads for the selected subtypes, and external capacitive loads for the selected subtypes.

11. The method of claim 9 wherein a decision to merge the selected subtypes is made by comparing the distance between the two selected subtypes to a threshold value.

12. The method of claim 11 wherein the threshold value represents a tradeoff between the objective function and the cost.

13. The method of claim 12 further comprising adjusting the threshold value to change the balance between the objective function and the cost.

14. The method of claim 11 wherein at least one of the selected subtypes corresponds to a fixed-size subtype, the threshold value to which the distance between the fixed-size subtype and others of the selected subtypes is compared being different than the threshold value employed for comparisons among the other selected subtypes.

15. The method of claim 1 wherein the objective function comprises at least one of area and power dissipation.

16. The method of claim 1 wherein the cost comprises at least one of a layout cost which represents at least one layout resource required to lay out a cell corresponding to the at least one cell type, and a verification cost which represents at least one verification resource required to test a cell corresponding to the at least one cell type.

17. The method of claim 1 wherein the merging of the selected subtypes is performed with reference to at least one internal characteristic of the selected subtypes.

18. The method of claim 17 wherein the at least one internal characteristic comprises transistor sizes.

19. The method of claim 1 wherein the merging of the selected subtypes is performed with reference to at least one external characteristic of the selected subtypes.

20. The method of claim 19 wherein the at least one external characteristic comprises at least one of external resistive loads for the selected subtypes, and external capacitive loads for the selected subtypes.

21. The method of claim 1 further comprising, prior to sizing the transistors, partitioning the cell instances for each cell type into the first plurality of subtypes.

22. The method of claim 21 wherein the partitioning of the cell instances comprises making subtype assignments for parent cell instances on a first level of a hierarchy of the circuit design with reference to a number of parent cell subtypes, and estimated subtype counts for child cell instances in the parent cell instances on at least one other level of the hierarchy below the first level.

23. The method of claim 22 wherein each of the subtype assignments for the parent cell instances is made with reference to a profit function representing a profit corresponding to the subtype assignment.

24. The method of claim 23 wherein the profit function relates an area gain for a given number of subtypes for the parent cell instances to a layout cost associated with the given number of subtypes.

25. The method of claim 21 wherein the circuit design corresponds to a hierarchy having a word level, and wherein partitioning the cells instances for each cell type into the first plurality of subtypes comprises partitioning all cell instances corresponding to the word level and any level of the hierarchy below the word level.

26. The method of claim 25 further wherein cell instances contained in arrays are excluded from the partitioning.

27. The method of claim 1 further comprising mapping the first plurality of subtypes into a metric space which relates the objective function and the cost.

28. The method of claim 27 further comprising weighting each of the first plurality of subtypes in accordance with a number of the cell instances corresponding thereto.

29. The method of claim 1 wherein the sizing of the transistors comprises:

generating a set of paths between observable nodes in a netlist representing the circuit design, each path corresponding to a sequence of signal transitions; and

sizing transistors represented in the netlist to attempt to meet a delay constraint for each path, the delay constraint corresponding to a unit delay times the number of signal transitions in the corresponding path, a plurality of individual delays of different durations

being allocated among the transitions for at least one of the paths to meet the delay constraint, at least one of the individual delays exceeding the unit delay.

30. An integrated circuit designed according to the method of claim 1.

31. At least one computer readable medium having data structures stored therein representing a sized netlist generated according to the method of claim 1.

32. A set of semiconductor processing masks generated using a sized netlist generated according to the method of claim 1.

33. At least one computer-readable medium having computer program instructions stored therein which are operable to perform the method of claim 1.

34. An electronic system comprising at least one integrated circuit designed according to the method of claim 1.